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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Paper No. 33

Application Number: 09/045,041

Filing Date: March 20, 1998

Appellant(s): Fujisawa

Christine Joan Gilsdorf

<u>For Appellant</u>

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/22/2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect, for the following reasons:

- The Yokomizo et al., Filseth and Shinsha rejections are withdrawn in order to simplify the issues before the Board.

- The Hachiya, Wang et al., and Kuehlmann et al. rejections are withdrawn in view of Appellants arguments.

- The Examiner has reconsidered the material recited in claims 19, 31, 43. A correct statement of the status of the claims is as follows:

Claims 9-12, 14-18, 20-24, 26-30, 32-36, 38-42, 44 are finally rejected (102 under Chakrabarti et al.)

Claims 19, 31, 43 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments *after final rejection* contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is not agreed with for the following reasons. Appellants have provided voluminous recitations of their invention as read from the specification but have not specifically mapped the claims to the "*Summary of the Invention*". MPEP section 1200 recites, in part:

> Summary of Invention. A concise explanation of the invention defined in the claims involved in the appeal. This explanation is required to refer to the specification by page and line number, and, if there is a drawing, to the drawing by reference characters. Where applicable, ***it is preferable to read the appealed claims on the specification and any drawing***. While reference to page and line number of the specification may require somewhat more detail than simply summarizing the invention, ***it is considered important to enable the Board to more quickly determine where the claimed subject matter is described in the application.***

Furthermore, the Examiner objects to the commentary (i.e., second full paragraph, page 4, Brief to first full paragraph, page 5, Brief) which appears to be argumentative in nature and is irrelevant as it relates to "*Summary of the Invention*". Such commentary has not been considered. Finally, it is noted that most of the summary of the invention is directed at the "Quasi-Equivalence" feature. This is not actually claimed until claims 19, 31, 43, which are now objected to but would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct. However, note that only the Chakrabarti rejection is outstanding. Furthermore, Appellants appear to introduce argument by reference to "subissues". The Examiner only agrees that the issues are whether the claims have been properly rejected over the prior art.

(7) Grouping of Claims

The appellant's statement in the brief that certain claims do not stand or fall together is not agreed with because Appellant's brief does not include a statement that this grouping of claims does not stand or fall together and ***reasons in support thereof***. See 37 CFR 1.192(c)(7). Furthermore, Appellants have not actually argued *any* of the claims on pages 8-13 of the Appeal Brief (paper # 31); Appellants have instead have only referred to the prior art without referring to any of the claims. Appellants only refer to claims 9, 21 and 33 on page 7 of the Brief. It is apparent from the argument on page 7 of the Brief that there is no alleged patentable distinction between claims 9, 21 and 33 (Paragraph 3 also states,

"Similar to claim 9, claim 21 ...."; Furthermore, note the last two paragraphs on page 7 and the apparent similarity in the arguments). The only argument for the dependent claims is (pg. 13, Appeal Brief) that "*The dependent claims depend from the above-discussed independent claims and are patentable over the prior art for at least the reasons discussed above*".

Section 1200 provides guidance:

(7) Grouping of Claims. For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone, unless a statement is included that the claims of the group do not stand or fall together and, in the argument section of the brief (37 CFR 1.192(c)(8)), appellant explains why the claims of the group are believed to be separately patentable. ***Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable***. If an appealed ground of rejection applies to more than one claim and appellant considers the rejected claims to be separately patentable, 37 CFR 1.192(c)(7) requires appellant to state that the claims do not stand or fall together, ***and to present in the appropriate part or parts of the argument under*** 37 CFR 1.192(c)(8) the reasons why they are considered separately patentable. The absence of such a statement ***and argument*** is a concession by the applicant that, if the ground of rejection were sustained as to any one of the rejected claims, it will be equally applicable to all of them. 37 CFR 1.192(c)(7) is consistent with the practice of the Court of Appeals for the Federal Circuit indicated in such cases as In re Young, 927 F.2d 588, 18 USPQ2d 1089 (Fed. Cir. 1991); In re Nielson, 816 F.2d 1567, 2 USPQ2d 1525 (Fed. Cir. 1987); In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); and In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983). 37 CFR 1.192(c)(7) requires the inclusion of reasons in order to avoid unsupported assertions of separate patentability. The reasons may be included in the appropriate portion of the "Argument" section of the brief. For example, if claims 1 to 4 are rejected under 35 U.S.C. 102 and appellant considers claim 4 to be separately patentable from claims 1 to 3, he or she should so state in the "Grouping of claims" section of the brief, and then give the reasons for separate patentability in the 35 U.S.C. 102 portion of the "Argument" section (i.e., under 37 CFR 1.192(c) (8) (iii)). In the absence of a separate statement that the claims do not stand or fall together, the Board panel assigned to the case will normally select the broadest claim in a group and will consider only that claim, even though the group may contain two broad claims, such as "ABCDE" and "ABCDF.". The same would be true in a case where there are both broad method and apparatus claims on appeal in the same group. ***The rationale behind the rule, as amended, is to make the appeal process as efficient as possible***. Thus, while the Board will consider each separately argued claim, the work of the Board can be done in a more efficient manner by selecting a single claim from a group of claims when the appellant does not meet the requirements of 37 CFR 1.192(c)(7). It should be noted that 37 CFR 1.192(c)(7) requires the appellant to perform two affirmative acts in his or her brief in order to have the separate patentability of a plurality of claims subject to the same rejection considered. The appellant must (A) state that the claims do not stand or fall together and (B) present arguments why the claims subject to the same rejection are separately patentable. Where the appellant does neither, the claims will be treated as standing or falling together. Where, however, the appellant (A) omits the statement required by 37 CFR 1.192(c)(7) yet presents arguments in the argument section of the brief, or (B) includes the statement required by 37 CFR 1.192(c)(7) to the effect that one or more claims do not stand or fall together (i.e., that they are separately patentable) yet does not offer argument

in support thereof in the "Argument" section of the brief, the appellant should be notified of the noncompliance as per 37 CFR 1.192(d). Ex parte Schier, 21 USPQ2d 1016 (Bd. Pat. App. & Int. 1991); Ex parte Ohsumi, 21 USPQ2d 1020 (Bd. Pat. App. & Int. 1991).

Appellants have never argued the claims as other than a single group.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

Chakrabarti et al. "An Improved Hierarchical Test Generation Technique for Combinational Circuits with Repertative Sub-circuits" IEEE Proc. Fourth Test Symp., (1995), pp. 237-243.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 9-12, 14-18, 20-24, 26-30, 32-36, 38-42, 44 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Chakrabarti et al..

(11) Response to Argument

Chakrabarti et al. disclose "*An improved hierarchical test generation technique for combinational circuits with repetitive sub-circuits.*" They also disclose an ***improved hierarchical testing algorithm for combinational circuits with repetitive sub-circuits using the bus fault model. This model exploits the regularity of a circuit by grouping together identical gate-level sub-circuits into high-level sub-circuits***. Though the existing test generation techniques using this model reduces the required time substantially in many cases, it fails on encountering

incompatibility between the inputs and outputs of high-level modules. The algorithm proposed helps in resolving high level incompatibility. The concept of a state transition graph has been used and it has been shown that resolving incompatibility at the high level is equivalent to finding a loop in the state transition graph. ***The technique is hierarchical in the sense that the original modeled high-level circuit is sub-divided into a number of components as soon as an incompatibility is encountered***. The results of implementation of the algorithm for a class of combinational circuits indicate a significant reduction in the test generation time and complete fault coverage thus validating our technique. See section 4.

Referring to claim 9, for example, Chakrabart et al. disclose

- inputting configuration data (abstract; "An ***improved hierarchical testing algorithm for combinational circuits with repetitive sub-circuits using the bus fault model. This model exploits the regularity of a circuit by grouping together identical gate-level sub-circuits into high-level sub-circuits***.");

- extracting partial circuits to inspect (abstract; "An ***improved hierarchical testing algorithm for combinational circuits with repetitive sub-circuits using the bus fault model. This model exploits the regularity of a circuit by grouping together identical gate-level sub-circuits into high-level sub-circuits***.");

- detecting partial circuits with equivalent operational characteristics (abstract; "An ***improved hierarchical testing algorithm for combinational circuits with repetitive sub-circuits using the bus fault model. This model exploits the regularity of a circuit by grouping together***

identical gate-level sub-circuits into high-level sub-circuits."; "the modeled high-level circuit is sub-divided into a number of components as soon as an incompatibility is encountered");

- compressing the partial circuits with equivalent operational characteristics and simulating the compressed circuit (abstract; "An ***improved hierarchical testing algorithm for combinational circuits with repetitive sub-circuits using the bus fault model. This model exploits the regularity of a circuit by grouping together identical gate-level sub-circuits into high-level sub-circuits***.".).

Appellants argue (pages 9-10, Appeal Brief) that the patentable discntion between Chakrabarti et al. and the claimed invention is:

> "The Chakrabarti reference discloses a hierarchical test pattern generation technique for combinational circuits with repetitive sub-circuits, in which the regularity of one circuit is exploited by ***grouping together identical gate-level sub-circuits into high-level sub-circuits based upon the characteristics of logical operations***. In Chakrebarti, a hieracrhical test pattern is generated at high speed using a circuit model with the high-level sub-circuits. See Chalrabari at abstract.
>
> In contrast, in the present invention, circuit simulation is performed by integrating a plurality of partial circuits that are determined to exhibit equivalent operational characteristics into one partial circuit."

(Emphasis added).

Appellants then conclude that Chakrabarti does not teach or suggest the claimed invention.

The Examiner respectfully, would like to point out that "***grouping together identical gate-level sub-circuits into high-level sub-circuits based upon the <u>characteristics of logical operations</u>***" ***is equivalent*** to "integrating a plurality of partial circuits that are determined to

exhibit equivalent operational characteristics into one partial circuit." *Logical operations* in a *logic device* refers to *operational behavior*.

(12) Concluding Remarks

The Examiner notes that Appellants have not explained the patentable distinction of the claimed invention. The Board is cordially invited to review the prosecution history to determine whether Appellants have made persuasive arguments throughout the prosecution.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Hugh Jones HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Primary Patent Examiner

December 6, 2001

Conferees

Kevin Teska

William Thomson